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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/401,070	09/22/1999	ARTHUR ANDERSON	3876	4148

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EXAMINER
RYMAN, DANIEL J

ART UNIT	PAPER NUMBER
2665	11

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/401,070	ANDERSON ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment., See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 55 is rejected under 35 U.S.C. 102(b) as being anticipated by Jones (USPN 5,140,611).

3. Regarding claim 55, Jones discloses a method for assigning a bit value of one or zero to a data bit having a high portion and a low portion within a single bit period, the method comprising the steps of receiving the data bit; measuring a width of either the high portion or the low portion of the data bit within the single bit period; and assigning a bit value of one to the data bit if the width measured falls within a first predetermined range or assigning a bit value of zero to the data bit if the width measured falls within a second predetermined range (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1-3, 14-16, 26, 27, 33, 40, 45, 56-58, 60, 61, 66, 70, 71, 75, and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360).

6. Regarding claims 1, 14, 15, 26, 33, 66, 70, and 75, Endick discloses a telecommunication system comprising: a telephone handset (ref. 106 and col. 3, lines 4-13); an accessory adapter (option bus and microcontroller) coupled to the telephone handset and having an accessory interface bus (option bus) for transmitting and receiving communications packets (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38) where the accessories include a headset attachment (col. 3, lines 66-68); a micro-controller coupled to the interface bus (ref. 118; col. 3, lines 27-36; and col. 5, lines 22-42), for controlling and monitoring at least one accessory to the telecommunications headset which is coupled to the interface bus (col. 3, lines 27-36 and col. 5, lines 22-42), wherein the micro-controller controls and monitors the accessory through the bi-directional transmission of communications packets between the micro-controller and the accessory via the interface bus (col. 3, lines 27-36 and col. 5, lines 22-42) with one purpose being to test the headset accessory and verify proper operation of the headset accessory (col. 8, lines 7-10); and an accessory for the telephone headset coupled to the accessory interface bus of the headset adapter, wherein the accessory can be directly controlled or monitored by the headset adapter via the transmission of communications packets between the accessory and the headset adapter over the accessory interface bus (col. 3, lines 4-14; col. 3, line 27-36; col. 3, line 58-col. 4, line 10; col. 5, lines 22-42; and col. 8, lines 15-29). Endick possibly does not disclose that the telecommunication system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick does disclose having an accessory interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick also discloses that

these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset.

7. Regarding claims 2, 71, and 76, referring to claims 1, 70, and 75, Endick discloses that the accessory interface bus includes at least one bi-directional signaling line for transmitting and receiving the communications packets between the accessory and the headset adapter in order to control or monitor the accessory (col. 8, lines 15-29).

8. Regarding claims 3, 16, and 27, referring to claims 1, 15, and 26, Endick discloses that the accessory interface bus further includes: a power bus containing lines for +/- 5V and +/- VAUX (col. 3, lines 58-60 and col. 5, lines 43-48) where the +5V and +VAUX is broadly defined as a high voltage rail and the –5V and –VAUX is broadly defined as a low voltage rail; and at least one bi-directional signaling line for transmitting and receiving communications packets between the accessory and the headset adapter in order to control or monitor the accessory (col. 8, lines 15-29).

9. Regarding claim 40, Endick discloses a method for controlling or monitoring an accessory to a telecommunications handset using an accessory adapter base and an interface bus, the method comprising: detecting whether an accessory is coupled to the interface bus (polling) (col. 8, lines 15-29); and transmitting a command or status request signal from the adapter base over the interface bus and to the accessory in order to control or monitor operation of the accessory (col. 8, line 15-col. 9, line 36). Endick does not disclose that the telecommunication

system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick does disclose having an accessory interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick also discloses that these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset.

10. Regarding claim 45, referring to claim 40, Endec discloses receiving a response signal from the accessory returning information on the current status of the accessory when a status request signal is transmitted (col. 8, line 15-col. 9, line 36).

11. Regarding claim 56, Endick discloses a communications protocol for an accessories interface bus comprising a plurality of commands to control, monitor, or identify any one of a plurality of accessories coupled to the interface bus (col. 8, line 15-col. 9, line 36). Endick does not disclose that the accessories interface bus is a telephone headset accessories interface bus; however, Endick does disclose having a headset accessory on the bus in addition to other accessories (col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). Since the bus can be used for a headset accessory in addition to other accessories, it would have been obvious to one of ordinary skill in the art to have the accessories bus be a telephone headset

accessories bus in order to allow the telephone user to use a telephone headset along with associated accessories.

12. Regarding claim 57, referring to claim 56, Endick discloses that the plurality of commands include common commands for controlling and monitoring any one of the plurality of accessories and accessory specific commands for controlling and monitoring a specific accessory in the plurality of accessories (col. 8, line 15-col. 9, line 36).

13. Regarding claim 58, referring to claim 57, Endick discloses that the common commands include: a command for polling the interface bus and detecting each of the plurality of accessories (col. 8, line 15-col. 9, line 36); and a command for resetting each of the plurality of accessories (col. 8, lines 59-68).

14. Regarding claim 60, referring to claim 57, Endick discloses that the accessory specific commands include: a command for turning the specific accessory on or off (col. 7, line 56-col. 8, line 14, esp. col. 7, lines 59-63); a command for resetting the specific accessory (col. 8, lines 59-68); and a command for requesting the status of the specific accessory (col. 7, line 56-col. 8, line 14, esp. col. 8, lines 7-10).

15. Regarding claim 61, referring to 57, Endick possibly does not expressly disclose that the accessory specific commands include a command for simulating a button press of the specific accessory; however, Endick does suggest this by disclosing that an option can be turned on remotely (col. 7, lines 59-63) where it is obvious that an option typically have a power switch located on the device itself. In addition, remote control is very well known in the art as a means to allow a user to control a device without being in physical contact with the device. It would have been obvious to one of ordinary skill in the art at the time of the invention to use utilize

remote control in order to allow a user to remotely control an accessory from the base such that the user is able to control the accessory without being in physical contact with the accessory.

16. Claims 4-6, 17-19, 28, 29, 34, 35, 41, 46, 72-74, and 77-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claims 1, 15, 26, 33, 40, 45, 70, and 75 above, and further in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488).

17. Regarding claims 4, 17, 28, 34, 41, 46, 72, and 77, referring to claims 1, 15, 26, 33, 40, 45, 70, and 75, Endick possibly does not expressly disclose that each communications packet includes a synch pulse which defines a transmission rate for the communications packet. Yamaguchi discloses, in a bi-directional communication system, having a synch pulse contained in each packet (col. 8, lines 10-15 where a frame and a packet can be viewed as being analogous). Yamaguchi further discloses that synch pulses are well known in the art (col. 10, lines 9-14). Typically a synch pulse is used in order to ensure that the transmitter and receiver have the same clock signal. If there is a mismatch in clocking, the receiver may not sample fast enough (sample for the wrong transmission rate) or it may sample at the wrong time periods such that the receiver will not be able to properly read a transmitted signal, as is evidenced by King (col. 2, lines 10-39). It is also obvious that such a system would allow for a variety of transmission rates to be used such that each accessory defines its own transmission rate using the synch pulse. It would have been obvious to one of ordinary skill in the art of packet communications to include a synch pulse which defines a transmission rate for the communications packet to ensure that the receiver will properly sample the incoming signal.

18. Regarding claims 5, 18, 29, 35, 73, and 78, referring to claims 4, 17, 28, 34, 72, and 77, Endick in view of Yamaguchi in further view of King discloses that the synch pulse includes a bit having a bit period which defines the synchronization for the communications packet (King: col. 1, line 64-col. 2, line 39, esp. col. 2, lines 31-39). It is obvious that in order to achieve bit synchronization, the transmission rate needs to be determined so that the receiver will know when to expect the next bit and so when to sample the transmitted signal. Endick in view of Yamaguchi in further view of King implements synchronization with a rate bit in order to minimize the amount of hardware used to generate the transmitted signal (King: col. 1, line 64-col. 2, line 6). It would have been obvious to one of ordinary skill in the art of packet communications to have the synch pulse include a rate bit having a bit period which defines the transmission rate for the communication packet in order to minimize the amount of hardware used to generate the transmitted signal.

19. Regarding claims 6, 19, 74, and 79, referring to claims 5, 18, 73, and 78, Endick in view of Yamaguchi in further view of King discloses that the rate bit includes a rising edge and a falling edge within the bit period (King: col. 2, lines 24-28) and that a duration of time between the rising edge and the falling edge is used to determine the bit period (King: col. 2, lines 24-28) where "equally spaced signal level transitions occur during each address bit period so as to thereby define a plurality of data bit periods in each address bit period" is taken to mean that the duration between a rising and falling edge (equally spaced signal level transitions) is used to determine a bit period (define a data bit period). Endick in view of Yamaguchi in further view of King possibly does not expressly state that the bit period is inversely related to the transmission

rate of the communications packet; however, it is well known in the art that a bit period is defined to be the inverse of the transmission rate.

20. Claims 7, 8, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) as applied to claims 5 and 17 above, and further in view of Miesterfeld et al (USPN 4,706,082).

21. Regarding claims 7 and 20, referring to claims 5 and 17, Endick in view of Yamaguchi in further view of King possibly does not disclose that the synch pulse holds the accessory bus at a predetermined level for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets. Miesterfeld discloses, in a system using a serial data bus, having in every packet start bits, which are used by a detector to determine if another transmitter has started to transmit almost simultaneously, so that collisions due to an almost simultaneous transmission are avoided (col. 5, lines 23-39). These start bits occur at the beginning of the message and it would be obvious to include the start bits in the synch pulse which also comes at the beginning of the message. Also because the start bits are used to indicate a beginning of a message and aid in determining if there is a collision, it would be obvious to locate the start bits before the rate bit, which is an important part of the message and so should be sent only after it is determined that the bus is clear. Thus it would have been obvious to one of ordinary skill in the art of communications to have the synch pulse hold the bus at a predetermined level (have start bits) for a predetermined amount of time before the rate bit of the communications packet is

transmitted over the accessory bus thereby preventing collision between communications packets.

22. Regarding claim 8, referring to claim 7, Endick in view of Yamaguchi in further view of King in further view of Miesterfeld possibly does not expressly disclose that the synch pulse holds the accessory interface bus to a low voltage value for at least two bit periods before the rate bit is transmitted in order to prevent collision between communications packets. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of critically in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The length of the duration and the value of the start bits are not critical to the operation of the disclosed system, and therefore it would be obvious to use any number of bit periods or any value.

23. Claims 9, 10, 21, 22, 30, 31, 36, 37, 43, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claims 1, 15, 26, 33, 40, and 45 above, and further in view of Waechter et al (USPN 4,943,963).

24. Regarding claims 9, 21, 30, 36, and 47, referring to claims 1, 15, 26, 33, and 45, Endick discloses that a slave select line is used to address a packet to an accessory (col. 5, lines 33-35) and that each option contains an ID (address) (col. 8, lines 44-46). Endick possibly does not

disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet; however, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art and would allow the elimination of slave select lines within Endick's system. In further regards to claim 30, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of critically in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The length of the destination address is not deemed essential to the operation of the disclosed interface bus, and so it would be obvious to have the address be any length including a byte.

25. Regarding claims 10, 22, 31, 37, and 43, referring to claims 9, 21, 30, 36, and 40, Endick in view of Waechter discloses that the communications packet further includes a checksum for

detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

26. Claims 11-13, 23-25, 32, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claims 1, 15, 26, and 33 above, and further in view of Jones et al (USPN 5,140,611).

27. Regarding claims 11 and 23, referring to claims 1 and 15, Endick discloses that each communications packet includes a plurality of bits with each bit in the plurality of bits having an assigned value of zero or one (col. 5, lines 22-25). Endick possibly does not disclose that each bit includes a first signal portion having a first logic level and a second signal portion having a second logic level and the assigned value of zero or one is assigned to each bit based upon a duration of either the first signal portion or the second signal portion. Jones teaches, in a communication system, (Fig. 2; col. 2, lines 34-52; col. 2, lines 61-67; and col. 5, lines 36-44) in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each bit includes a first signal portion having a first logic level and a second signal portion having a second logic level and the assigned value of zero or one is assigned to each bit based upon a duration of either the first signal portion or the second signal portion in order to have a data stream which is self-clocking.

28. Regarding claims 12 and 24, referring to claims 11 an 23, Endick in view of Jones discloses that if the duration of the at least one portion falls within a first range the bit is assigned a value of zero and if the duration of the at least one portion falls within a second range, the bit is assigned a value of one (Jones: Fig. 2; col. 2, lines 34-52; col. 2, lines 61-67; and col. 5, lines 36-44).

29. Regarding claims 13 and 25, referring to claims 11 and 23, Endick in view of Jones discloses that each bit in the plurality of bits has a rising edge and a falling edge, and the rising edge and the falling edge are used to synchronize transmission of the communications packet after each bit is transmitted (Jones: Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53).

30. Regarding claims 32 and 38, referring to claims 26 and 33, Endick possibly does not expressly disclose that each communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted. Jones discloses, in a communication system, having each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53). Jones does this in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted in order to have a data stream which is self-clocking.

31. Regarding claim 39, referring to claim 38, Endick in view of Jones discloses that each bit in the plurality of bits has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge can be used to synchronize transmission of the communications packet after each bit period (Jones: Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53).

32. Claims 42, 44, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) as applied to claims 41 and 46 above, and further in view of Waechter et al (USPN 4,943,963).

33. Regarding claim 42, referring to claim 41, Endick in view of Yamaguchi in further view of King discloses that a slave select line is used to address a packet to an accessory (Endick: col. 5, lines 33-35) and that each option contains an ID (address) (Endick: col. 8, lines 44-46) and communicating a slave address (Yamaguchi: col. 3, lines 32-35). Endick in view of Yamaguchi in further view of King possibly does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet; however, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit

the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art.

34. Regarding claim 44, referring to claim 42, Endick in view of Yamaguchi in further view of King in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

35. Regarding claim 48, referring to claim 46, Endick in view of Yamaguchi in further view of King possibly does not expressly disclose that the communications packet further includes a checksum for detecting errors in transmission of the communications packet from the accessory to the adapter base; however, using a checksum to detect errors in a communications packet is well known in the art, as is evidenced by Waechter (col. 5, lines 25-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to have a checksum in order to ensure that the packet was transmitted properly.

36. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claim 40 above, and further in view of Miesterfeld et al (USPN 4,706,082).

37. Regarding claim 49, referring to claim 40, Endick possibly does not disclose that the synch pulse holds the accessory bus at a predetermined level for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets. Miesterfeld discloses, in a system using a serial data bus, having in every packet start bits, which are used by a detector to determine if another transmitter has started to transmit almost simultaneously, so that collisions due to an

almost simultaneous transmission are avoided (col. 5, lines 23-39). These start bits occur at the beginning of the message and it would be obvious to include the start bits in the synch pulse which also comes at the beginning of the message. Also because the start bits are used to indicate a beginning of a message and aid in determining if there is a collision, it would be obvious to locate the start bits before the rate bit, which is an important part of the message and so should be sent only after it is determined that the bus is clear. Thus it would have been obvious to one of ordinary skill in the art of communications to have the synch pulse hold the bus at a predetermined level (have start bits) for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets.

38. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) as applied to claim 41 above, and further in view of Jones et al (USPN 5,140,611).

39. Regarding claim 50, referring to claim 41, Endick in view of Yamaguchi in further view of King possibly does not disclose that the communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are be used to synchronize transmission of the command or status request signal after each bit is transmitted. Jones discloses, in a communication system, having each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single

communications packet after each bit is transmitted (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53). Jones does this in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted in order to have a data stream which is self-clocking.

40. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) in further view of Waechter et al (USPN 4,943,963).

41. Regarding claim 51, Endick discloses a data packet transmitted over an accessory interface bus having a number of devices coupled thereto for controlling, monitoring or testing the operations of a headset accessory coupled to the interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). Endick does not disclose that the telecommunication system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick does disclose having an accessory interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick also discloses that these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a

telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset. Endick also possibly does not disclose that the data packet comprises: a synch pulse having a rate bit that defines a rate at which the data packet is being transmitted. Yamaguchi discloses, in a bi-directional communication system, having a synch pulse contained in each packet (col. 8, lines 10-15 where a frame and a packet can be viewed as being analogous. Yamaguchi further discloses that synch pulses are well known in the art (col. 10, lines 9-14). Typically a synch pulse is used in order to ensure that the transmitter and receiver have the same clock signal. If there is a mismatch in clocking, the receiver may not sample fast enough (sample for the wrong transmission rate) or it may sample at the wrong time periods such that the receiver will not be able to properly read a transmitted signal, as is evidenced by King (col. 2, lines 10-39). It is also obvious that such a system would allow for a variety of transmission rates to be used such that each accessory defines its own transmission rate using the synch pulse. It would have been obvious to one of ordinary skill in the art of packet communications to include a synch pulse which defines a transmission rate for the communications packet to ensure that the receiver will properly sample the incoming signal. Endick in view of Yamaguchi in further view of King possibly does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet. Endick in view of Yamaguchi in further view of King discloses that a slave select line is used to address a packet to an accessory (Endick: col. 5, lines 33-35) and that each option contains an ID (address) (Endick: col. 8, lines 44-46) and

communicating a slave address (Yamaguchi: col. 3, lines 32-35). However, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art.

42. Regarding claim 52, referring to claim 51, Endick in view of Yamaguchi in further view of King in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

43. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) in further view of Waechter et al (USPN 4,943,963) as applied to claim 51 above, and further in view of Jones et al (USPN 5,140,611).

44. Regarding claims 53 and 54, referring to claim 51, Endick in view of Yamaguchi in further view of King in further view of Waechter possibly does not disclose that the communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are be used to synchronize transmission of the command or status request signal after each bit is transmitted. Jones discloses, in a

communication system, having each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53). Jones does this in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted in order to have a data stream which is self-clocking.

45. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claim 57 above, and further in view of Yamada (USPN 5,414,751).

46. Regarding claim 59, referring to claim 57, Endick possibly does not expressly disclose that the common commands include: a command for requesting a firmware version number from each accessory in the plurality of accessories. Yamada discloses, in a system comprising a base unit and an accessory (mobile) unit, having a command for requesting a firmware version number from each accessory in the plurality of accessories (col. 4, lines 20-32) in order to determine if the accessory needs an update of the firmware. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a command for requesting a firmware

version number from each accessory in the plurality of accessories in order to determine if the accessory needs an update of the firmware.

47. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claim 57 above, and further in view of Tanaka et al (USPN 5,003,536).

48. Regarding claim 62, referring to claim 57, Endick possibly does not expressly disclose that the accessory specific commands include: a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory. Tanaka discloses, in a system using a base (master) and accessory (slave), having a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory (col. 4, lines 1-29). Such a system is well known in the art in order to allow for distributed memory and in order to allow the accessory to store information relating to future communications with the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory in order to allow for distributed memory and in order to allow the accessory to store information relating to future communications with the controller.

49. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Tanaka et al (USPN 5,003,536) in further view of Yamada (USPN 5,414,751).

50. Regarding claim 63, Endick discloses a combination comprising: an interface bus having an accessories adapter base and a plurality of accessories for the base coupled to the interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38), and a communications protocol for controlling and monitoring operations of the headset adapter base and the plurality of accessories (col. 8, line 15-col. 9, line 36), the communications protocol including at least one command selected from the group of commands consisting of: a command for turning an accessory on or off (col. 7, line 56-col. 8, line 14, esp. col. 7, lines 59-63); a command for polling the interface bus in order to determine what accessories are coupled to the interface bus (col. 8, line 15-col. 9, line 36); a command for resetting an accessory (col. 8, lines 59-68); a command for determining the status of an accessory (col. 7, line 56-col. 8, line 14, esp. col. 8, lines 7-10); and a command for determining the identity of each accessory (col. 8, lines 44-46). Endick does not disclose that the accessories interface bus is a telephone headset accessories interface bus; however, Endick does disclose having a headset accessory on the bus in addition to other accessories (col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). Since the bus can be used for a headset accessory in addition to other accessories, it would have been obvious to one of ordinary skill in the art to have the accessories bus be a telephone headset accessories bus in order to allow the telephone user to use a telephone headset along with associated accessories. Endick possibly does not expressly disclose that the accessory specific commands include a command for simulating a button press of the specific accessory or base; however, Endick does suggest this by disclosing that an option can be turned on remotely (col. 7, lines 59-63) where it is obvious that an option typically have a power switch located on the device itself. In addition, remote control is very well known in the art as a means to allow a

user to control a device without being in physical contact with the device. It would have been obvious to one of ordinary skill in the art at the time of the invention to use utilize a remote control in order to allow a user to remotely control an accessory from the base or to control the base from an accessory device such that the user is able to control the accessory or base without being in physical contact with the accessory or base. Endick possibly does not disclose a command for reading from or writing to a memory structure within an accessory. Tanaka discloses, in a system using a base (master) and accessory (slave), having a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory (col. 4, lines 1-29). Such a system is well known in the art in order to allow for distributed memory and in order to allow the accessory to store information relating to future communications with the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory in order to allow for distributed memory and in order to allow the accessory to store information relating to future communications with the controller. Endick in view of Tanaka possibly does not expressly disclose a command for determining the version of each accessory. Yamada discloses, in a system comprising a base unit and an accessory (mobile) unit, having a command for requesting a firmware version number from each accessory in the plurality of accessories (col. 4, lines 20-32) in order to determine if the accessory needs an update of the firmware. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a command for requesting a firmware version number from each accessory in the plurality of accessories in order to determine if the accessory needs an update of the firmware.

51. Claims 64 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Tanaka et al (USPN 5,003,536) in further view of Yamada (USPN 5,414,751) as applied to claim 63 above, and further in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) in further view of Waechter et al (USPN 4,943,963).

52. Regarding claim 64, Endick in view of Tanaka in further view of Yamada discloses a data packet transmitted over an accessory interface bus having a number of devices coupled thereto for controlling, monitoring or testing the operations of a headset accessory coupled to the interface bus (Endick: Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). Endick in view of Tanaka in further view of Yamada does not disclose that the telecommunication system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick in view of Tanaka in further view of Yamada does disclose having an accessory interface bus (Endick: Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick in view of Tanaka in further view of Yamada also discloses that these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset. Endick in view of Tanaka in further view of Yamada also possibly does not disclose that the data packet comprises:

a synch pulse having a rate bit that defines a rate at which the data packet is being transmitted. Yamaguchi discloses, in a bi-directional communication system, having a synch pulse contained in each packet (col. 8, lines 10-15 where a frame and a packet can be viewed as being analogous. Yamaguchi further discloses that synch pulses are well known in the art (col. 10, lines 9-14). Typically a synch pulse is used in order to ensure that the transmitter and receiver have the same clock signal. If there is a mismatch in clocking, the receiver may not sample fast enough (sample for the wrong transmission rate) or it may sample at the wrong time periods such that the receiver will not be able to properly read a transmitted signal, as is evidenced by King (col. 2, lines 10-39). It is also obvious that such a system would allow for a variety of transmission rates to be used such that each accessory defines its own transmission rate using the synch pulse. It would have been obvious to one of ordinary skill in the art of packet communications to include a synch pulse which defines a transmission rate for the communications packet to ensure that the receiver will properly sample the incoming signal. Endick in view of Tanaka in further view of Yamada in view further view of Yamaguchi in further view of King possibly does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet. Endick in view of Tanaka in further view of Yamada in view further view of Yamaguchi in further view of King discloses that a slave select line is used to address a packet to an accessory (Endick: col. 5, lines 33-35) and that each option contains an ID (address) (Endick: col. 8, lines 44-46) and communicating a slave address (Yamaguchi: col. 3, lines 32-35). However, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication

system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art.

53. Regarding claim 65, referring to claim 64, Endick in view of Tanaka in further view of Yamada in further view of Yamaguchi in further view of King in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

54. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claim 66 above, and further in view of Tanaka et al (USPN 5,003,536) in further view of Yamada (USPN 5,414,751).

55. Regarding claim 67, referring to claim 66, Endick discloses that the at least one command is selected from the group of commands consisting of: a command for resetting an accessory (col. 8, lines 59-68); a command for determining the status of an accessory (col. 7, line 56-col. 8, line 14, esp. col. 8, lines 7-10); and a command for determining the identity of each accessory (col. 8, lines 44-46). Endick possibly does not expressly disclose that the accessory specific commands include a command for simulating a button press of the specific accessory or base; however, Endick does suggest this by disclosing that an option can be turned on remotely (col. 7, lines 59-63) where it is obvious that an option typically have a power switch located on the device itself. In addition, remote control is very well known in the art as a means to allow a user to control a device without being in physical contact with the device. It would have been obvious

to one of ordinary skill in the art at the time of the invention to use utilize a remote control in order to allow a user to remotely control an accessory from the base or to control the base from an accessory device such that the user is able to control the accessory or base without being in physical contact with the accessory or base. Endick possibly does not disclose a command for reading from or writing to a memory structure within an accessory. Tanaka discloses, in a system using a base (master) and accessory (slave), having a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory (col. 4, lines 1-29). Such a system is well known in the art in order to allow for distributed memory and in order to allow the accessory to store information relating to future communications with the controller. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a command for writing data to a memory within the specific accessory; and a command for reading data from a memory within the specific accessory in order to allow for distributed memory and in order to allow the accessory to store information relating to future communications with the controller. Endick in view of Tanaka possibly does not expressly disclose a command for determining the version of each accessory. Yamada discloses, in a system comprising a base unit and an accessory (mobile) unit, having a command for requesting a firmware version number from each accessory in the plurality of accessories (col. 4, lines 20-32) in order to determine if the accessory needs an update of the firmware. It would have been obvious to one of ordinary skill in the art at the time of the invention to have a command for requesting a firmware version number from each accessory in the plurality of accessories in order to determine if the accessory needs an update of the firmware.

56. Claims 68 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) as applied to claim 66 above, and further in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) in further view of Waechter et al (USPN 4,943,963).

57. Regarding claim 68, referring to claim 66, Endick possibly does not disclose a synch pulse having a rate bit that defines a rate at which the data packet is being transmitted. Yamaguchi discloses, in a bi-directional communication system, having a synch pulse contained in each packet (col. 8, lines 10-15 where a frame and a packet can be viewed as being analogous. Yamaguchi further discloses that synch pulses are well known in the art (col. 10, lines 9-14). Typically a synch pulse is used in order to ensure that the transmitter and receiver have the same clock signal. If there is a mismatch in clocking, the receiver may not sample fast enough (sample for the wrong transmission rate) or it may sample at the wrong time periods such that the receiver will not be able to properly read a transmitted signal, as is evidenced by King (col. 2, lines 10-39). It is also obvious that such a system would allow for a variety of transmission rates to be used such that each accessory defines its own transmission rate using the synch pulse. It would have been obvious to one of ordinary skill in the art of packet communications to include a synch pulse which defines a transmission rate for the communications packet to ensure that the receiver will properly sample the incoming signal. Endick in view of Yamaguchi in further view of King possibly does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet. Endick in view of Yamaguchi in further view of King discloses that a slave select line is used to address a packet to

an accessory (Endick: col. 5, lines 33-35) and that each option contains an ID (address) (Endick: col. 8, lines 44-46) and communicating a slave address (Yamaguchi: col. 3, lines 32-35). However, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art.

58. Regarding claim 69, referring to claim 66, Endick in view of Yamaguchi in further view of King in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

Response to Amendment

59. Applicant's arguments with respect to claims 1-79 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

60. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Acree (USPN 5,099,514) which discloses a headset adapter and base. Horiuchi et al (USPN 4,893,331) which discloses an telephone accessory adapter and base. Stelman (USPN 5,937,031) which discloses a handset interface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (703)305-6970. The examiner can normally be reached on Mon.-Fri. 7:00-5:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703)308-6602. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-6743 for regular communications and (703)308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Daniel J. Ryman
Examiner
Art Unit 2665

DJR

Daniel J. Ryman
April 3, 2003

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